



# CCDSC'14 Panel

Exascale topic

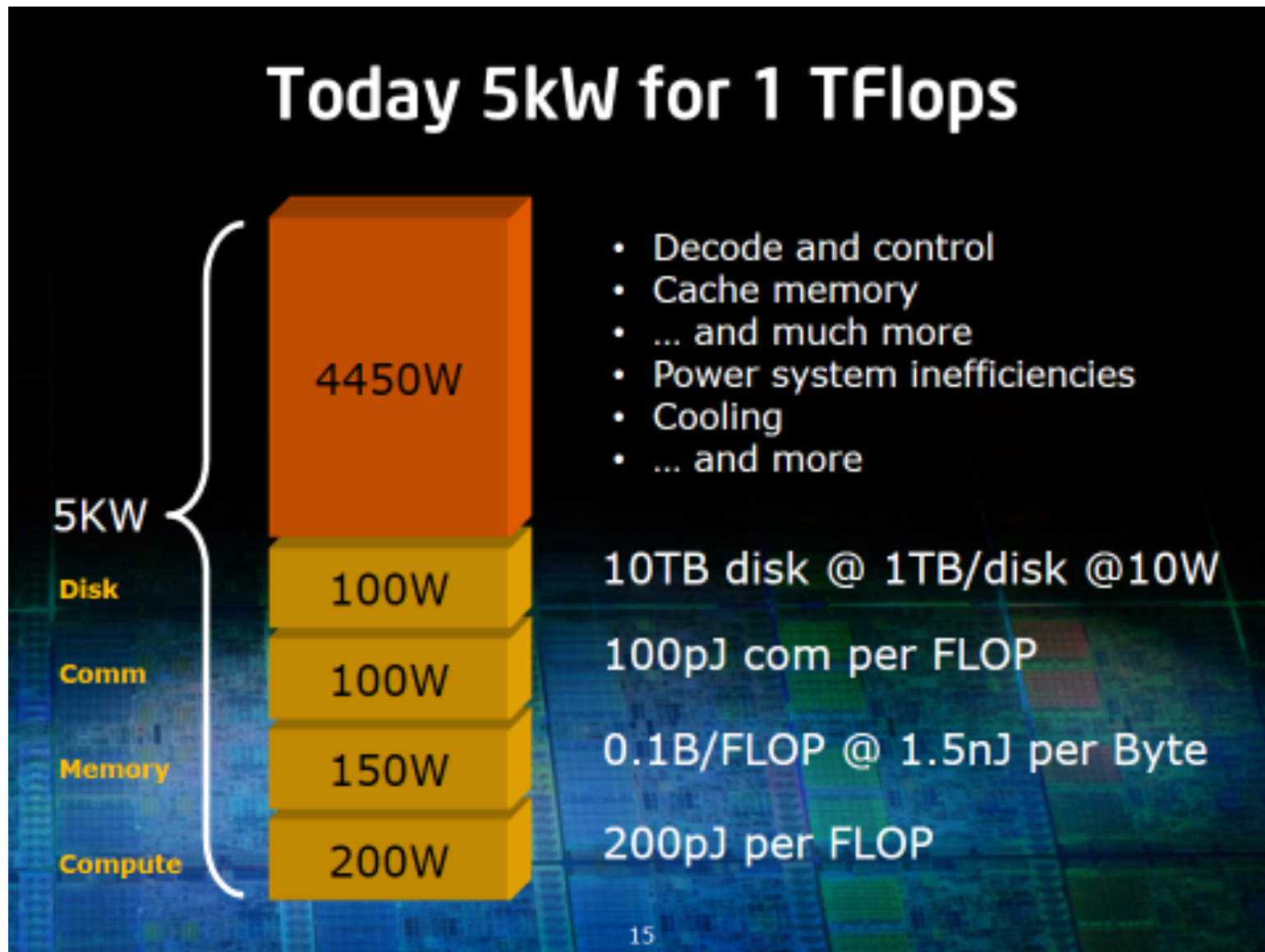
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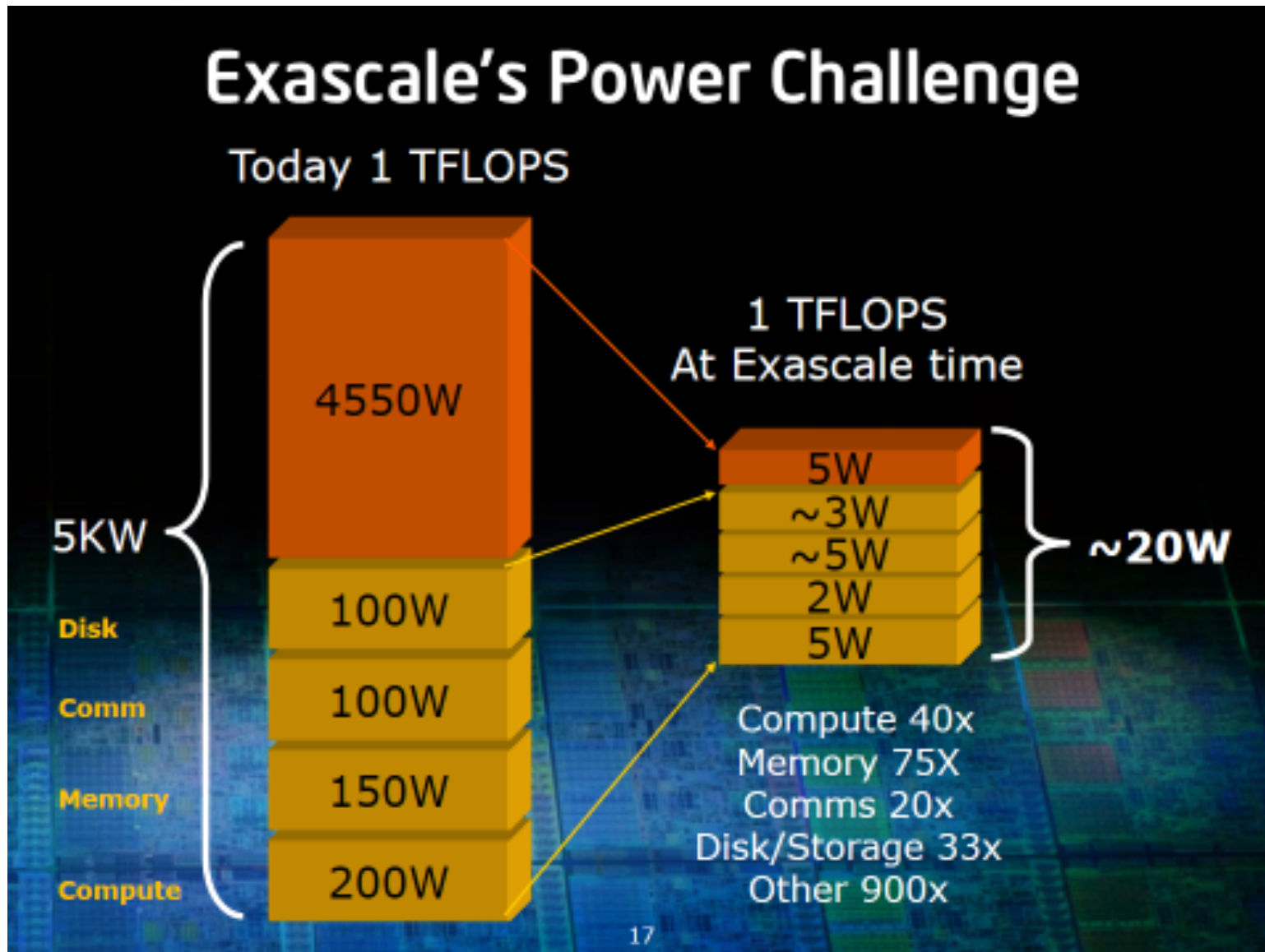
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# Problem statement (2011)



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# ExaFlops ???

1 EF (ExaFlops) =  $10^{18}$  Flops

How can we achieve this?

It ***\*could\**** take:

- A microarchitecture that does 10 ops/cycle  $10^1$
- In a core running at 2GHz  $2 \cdot 10^9$
- With 250 cores per socket  $2.5 \cdot 10^2$
- On a 200,000 sockets  $2 \cdot 10^5$

**One among many solutions**



# ExaFlops ???

1 EF (ExaFlops) =  $10^{18}$  Flops

How can we achieve this?

It ***\*could\**** take:

- A microarchitecture that does 10 ops/cycle  $10^1$
- In a core running at 2GHz  $2 \cdot 10^9$
- With 100 cores per socket  $10^2$
- On a 500,000 sockets  $5 \cdot 10^5$

**One among many solutions**

# ExaFlops ???

1 EF (ExaFlops) =  $10^{18}$  Flops

How can we achieve this?

It ***\*could\**** take:

- A microarchitecture that does 10 ops/cycle  $10^1$
- In a core running at 1GHz  $10^9$
- With 500 cores per socket  $5 \cdot 10^2$
- On a 200,000 sockets  $2 \cdot 10^5$

**One among many solutions**

# ExaFlops ???

1 EF (ExaFlops) =  $10^{18}$  Flops

How can we achieve this?

It ***\*could\**** take:

- A microarchitecture that does 10 ops/cycle  $10^1$
- In a core running at 1GHz  $10^9$
- With 1,000 cores per socket  $10^3$
- On a 100,000 sockets  $10^5$

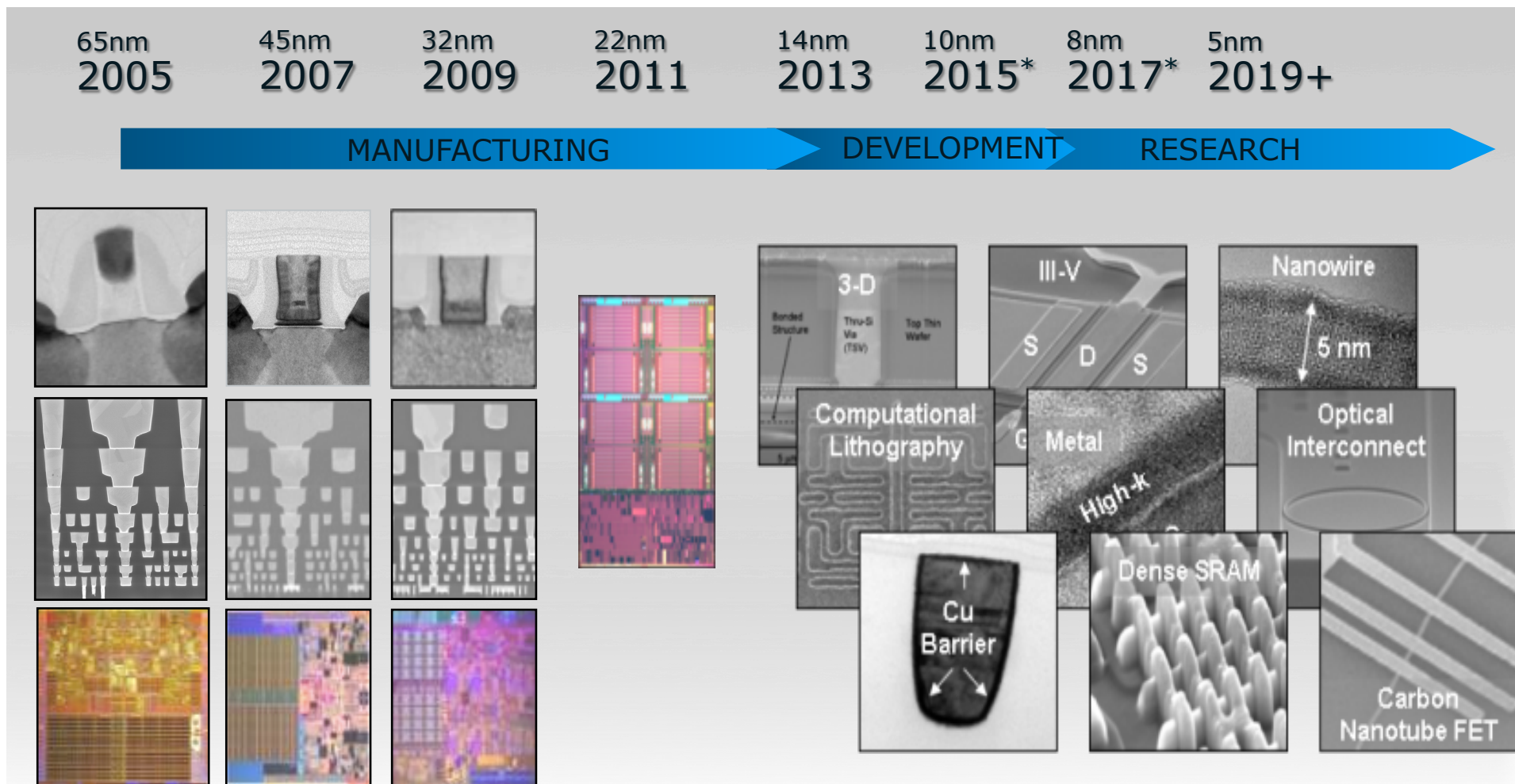
**One among many solutions**



# Today's Exascale Expectation



# Moore's Law



\* All products, dates, and figures specified are preliminary based on current expectations, and are subject to change without notice.

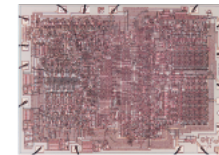
# Moore's Law - 22nm Tri-Gate

3<sup>rd</sup> Generation  
Intel® Core™  
Processor  
Family  
(2012, codename  
IvyBridge)

4004  
(1971)



VS.



4,000X Faster

5,000X Less Energy / Transistor

50,000X Cheaper / Transistor



Source: Intel

