Parallel computing models and their performances

A high level exploration of the HPC world

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Overview

• Definition of parallel application
• Architectures taxonomy
• What is quantifiable? Laws managing the parallel applications field
• Modeling performance of parallel applications
The **Bernstein Conditions** Let’s define:

- $I(P)$ all variables, registers and memory locations used by $P$
- $O(P)$ all variables, registers and memory locations written by $P$

Then $P_1; P_2$ is equivalent to $P_1 || P_2$ if and only if

$$\{I(P_1) \cap O(P_2) = \emptyset \& I(P_2) \cap O(P_1) = \emptyset \& O(P_1) \cap O(P_2) = \emptyset\}$$

**General case:** $P_1… P_n$ are parallel if and only if each for each pair $P_i, P_j$ we have $P_i || P_j$.

3 limit to the parallel applications:

1. **Data** dependencies
2. **Flow** dependencies
3. **Resources** dependencies
Data dependencies

I1: \( A = B + C \)
I2: \( E = D + A \)
I3: \( A = F + G \)

Flow dependency (RAW): a variable assigned in a statement is used in a later statement

Anti-dependency (WAR): a variable used in a statement is assigned in a subsequent statement

Output dependency (WAW): a variable assigned in a statement is subsequently re-assigned

How to avoid them?
Which type of data dependency can be avoided?
Flow dependencies

I1: \[ A = B + C \]
I2: \[ \text{if}( A ) \{ \]
I3: \[ D = E + F \} \]
I4: \[ G = D + H \]

--- Data dependency

--- Control dependency

How to avoid?
Resources dependencies

I1: \[ A = B + C \]
I2: \[ G = D + H \]

How to avoid?
A more complicated example (loop)

for i = 0 to 9
  A[i] = B[i]

All statements are independent, as they relate to different data. They are concurrent.

for i = 1 to 9
  A[i] = A[i-1]


All statements are dependent, as every 2 statements are strictly sequential.
Flynn Taxonomy (1966)

- Computers classified by instruction delivery mechanism and data stream(s)
  - I for instruction, P for program. Conceptually similar, technically at a different granularity.
- 4 characters code: 2 for instruction stream and 2 for data stream

<table>
<thead>
<tr>
<th></th>
<th>1 Instruction flow</th>
<th>&gt; 1 Instruction flow</th>
</tr>
</thead>
<tbody>
<tr>
<td>1 data stream</td>
<td>SISD, Von Neumann</td>
<td>MISD pipeline</td>
</tr>
<tr>
<td>&gt; 1 data stream</td>
<td>SIMD</td>
<td>MIMD</td>
</tr>
</tbody>
</table>
Flynn Taxonomy: Analogy

• **SISD**: assembly line work (no parallelism)
• **SIMD**: systolic, GPU computing (vector computing MMX, SSE, AVX)
• **MISD**: more unusual type. Safety requirements, replication capabilities, think space shuttle.
• **MIMD**: airport facility, several desks working at their own pace, synchronizing via a central entity (database). Most distributed algorithms, as well as multi-core applications.
Amdahl Law

• First law of parallel applications (1967)
• Limit the speedup for all parallel applications

\[
speedup = \frac{s + p}{N} = \frac{1}{a + \left(1 - a\right)/N}
\]
Amdahl Law

Speedup is bound by $1/a$. 

FIGURE 1. Speedup under Amdahl's Law
Amdahl Law

- Bad news for parallel applications
- 2 interesting facts:
  - We should limit the sequential part
  - A parallel computer should be a fast sequential computer to be able to resolve the sequential part quickly
- What about increasing the size of the initial problem?
Gustafson’s Law

- Less constraints than the Amdahl law.
- In a parallel program the quantity of data to be processed increase, so the sequential part decrease.

\[
\begin{align*}
t &= s + \frac{P}{n} \\
P &= an
\end{align*}
\]

\[
speedup = \frac{s + an}{s + a}
\]

\[
a \rightarrow \infty \Rightarrow speedup \rightarrow n
\]
Gustafson’s Law

- The limit of Amdahl Law can be transgressed if the quantity of data to be processed increase.

\[ speedup \leq n + (1 - n)s \]

Rule stating that if the size of most problems is scaled up sufficiently, then any required efficiency can be achieved on any number of processors.
Speedup

• Superlinear speedup?

Sometimes superlinear speedups can be observed!
  • Memory/cache effects
  • More processors typically also provide more memory/cache.
  • Total computation time decreases due to more page/cache hits.
• Search anomalies
  • Parallel search algorithms.
  • Decomposition of search range and/or multiple search strategies.
  • One task may be "lucky" to find result early.
Parallel execution models

- Amdahl and Gustafson laws define the limits without taking into account the properties of the computer architecture.
- They can only loosely be used to predict (in fact mainly to cap) the real performance of any parallel application.
- We should integrate in the same model the architecture of the computer and the architecture of the application.
What are models good for?

- Abstracting the computer properties
  - Making programming simple
  - Making programs portable?
- Reflecting essential properties
  - Functionality
  - Costs
- What is the von-Neumann model for parallel architectures?
Parallel Random Access Machine

- Specialized in parallel algorithms
  - **Natural**: the number of operations per cycle on N processors is at most N
  - **Strong**: all accesses are realized in a single time unit
  - **Simple**: keep the complexity and correctness overheads low by abstracting all communication or synchronization overheads

- World described as a collection of synchronous processors which communicate with a global shared memory unit.

The PRAM corresponds intuitively to the programmers' view of a parallel computer: it ignores lower level architectural constraints, and details, such as memory access contention and overhead, synchronization overhead, interconnection network throughput, connectivity, speed limits and link bandwidths, etc.
How to represent the architecture

• 2 resources have a major impact on the performances:
  • The couple (processor, memory)
  • The communication network.

• The application should be described using those 2 resources.

\[ T_{\text{app}} = T_{\text{comp}} + T_{\text{comm}} \]
Models

- 2 models are often used.
- They represent the whole system as composed by \( n \) identical processors, each of them having his own memory.
- They are interconnected with a predictable network.
- They can realize synchronizations.
Bulk Synchronous Parallel – BSP

- Distributed-memory parallel computer
- Global vision as a number of processor/memory pairs interconnected by a communication network

Each processor can access his own memory without overhead and have a uniform slow access to remote memory
BSP

- Applications composed by Supersteps separated by global synchronizations.

- One superstep include:
  - A computation step
  - A communication step
  - A synchronization step

Synchronization used to insure that all processors complete the computation + communication steps in the same amount of time.
BSP
\[ T_{\text{superstep}} = w + g \times h + l \]

Where:

- \( w \) = max of computation time
- \( g \) = \( 1/(\text{network bandwidth}) \)
- \( h \) = max of number of messages
- \( l \) = time for the synchronization

Sketch the communications
• An algorithm can be described using only $w$, $h$ and the problem size.

• Collections of algorithms are available depending on the computer characteristics.
  • Small L
  • Small g

• The best algorithm can be selected depending on the computer properties.
BSP - example

• Numerical solution to Laplace’s equation

\[
U_{i,j}^{n+1} = \frac{1}{4} \left( U_{i-1,j}^n + U_{i+1,j}^n + U_{i,j-1}^n + U_{i,j+1}^n \right)
\]

for \( j = 1 \) to \( j_{\text{max}} \)

for \( i = 1 \) to \( i_{\text{max}} \)

\[
\text{Unew}(i,j) = 0.25 \times ( U(i-1,j) + U(i+1,j) + U(i,j-1) + U(i,j+1) )
\]

end for

end for
BSP - example

- The approach to make it parallel is by partitioning the data
• The approach to make it parallel is by partitioning the data

Overlapping the data boundaries allow computation without communication for each superstep

On the communication step each processor update the corresponding columns on the remote processors.
for \( j = 1 \) to \( j_{\text{max}} \)
  for \( i = 1 \) to \( i_{\text{max}} \)
    \[
    u_{\text{new}}(i,j) = 0.25 \times (U(i-1,j) + U(i+1,j) + U(i,j-1) + U(i,j+1))
    \]
  end for
end for
if me not 0 then
  bsp\_put( to the left )
endif
if me not NPROCS - 1 then
  bsp\_put( to the right )
Endif
bsp\_sync()
BSP - example

\[ T_{\text{superstep}} = w + g \cdot h + l \]

\( h = \text{max number of messages} \)
\( = I \text{ values to the left} + I \text{ values to the right} \)
\( = 2 \cdot I \) (ignoring the inverse communication!)

\( w = 4 \cdot I \cdot I / p \)

\[ T_{\text{superstep}} = 4 \frac{I^2}{p} + 2 \cdot g \cdot I + l \]
BSP - example

- BSP parameters for a wide variety of architectures has been published.

<table>
<thead>
<tr>
<th>Machine</th>
<th>s</th>
<th>p</th>
<th>l</th>
<th>g</th>
</tr>
</thead>
<tbody>
<tr>
<td>Origin 2000</td>
<td>101</td>
<td>4</td>
<td>1789</td>
<td>10.24</td>
</tr>
<tr>
<td></td>
<td></td>
<td>32</td>
<td>39057</td>
<td>66.7</td>
</tr>
<tr>
<td>Cray T3E</td>
<td>46.7</td>
<td>4</td>
<td>357</td>
<td>1.77</td>
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<tr>
<td></td>
<td></td>
<td>16</td>
<td>751</td>
<td>1.66</td>
</tr>
<tr>
<td>Pentium 10Mbit</td>
<td>61</td>
<td>4</td>
<td>139981</td>
<td>1128.5</td>
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<td></td>
<td></td>
<td>8</td>
<td>826054</td>
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<tr>
<td>Pentium II</td>
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<td>4</td>
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<tr>
<td>100Mbit</td>
<td>8</td>
<td>8</td>
<td>38788</td>
<td>38.7</td>
</tr>
</tbody>
</table>
A more sophisticated model LogP

- Tend to be more empirical and network-related.
A more sophisticated model LogP

- Tend to be more empirical and network-related.
• Decompose the communications in 3 elements:
  • Latency: small message cross the network
  • Overhead: lost time in communication
LogP

- Decompose the communications in 3 elements:
  - Latency: small message cross the network
  - Overhead: lost time in communication
  - Gap: between 2 consecutive messages
- And P the number of processors.

Both \( g \) and \( o \) matter!

\[ g > o \quad \text{and} \quad g < o \]
LogP

• The total time for a message to go from the processor A to the processor B is:
  \[ L + 2 \times o \]

• There is no model for the application

• We can describe the application using the same approach as for BSP: supersteps

  \[ T_{\text{superstep}} = w + h \times (L + 2o) + l \]
LogP

• The P parameter does not interfere in the superstep computation?

• When the number of processors is not fixed:
  • The time of the computation change \( w(p) \)
  • The number of messages change \( h(p) \)
  • The synchronization time change \( l(p) \)
LogP

• Allow/encourage the usage of general techniques of designing algorithms for distributed memory machines: exploiting locality, reducing communication complexity and overlapping communication and computation.

• Balanced communication to avoid overloading the processors.
LogP

• Interesting concept: idea of finite capacity of the network. Any attempt to transit more than a certain amount of data will stall the processor.

\[
\begin{bmatrix}
L \\
g
\end{bmatrix}
\]

• This model does not address on the issue of message size, even the worst is the assumption of all messages are of ``small" size.

• Does not address the global capacity of the network.
Design a LogP program

• Execution time is the time of the slowest process

• Implications for algorithms:
  • Balance computation
  • Balance communications

  Are only sub-goals!

• Remember the capacity constraint

\[
\left[ \frac{L}{g} \right]
\]
LogP Machines

<table>
<thead>
<tr>
<th>Machine</th>
<th>$L$</th>
<th>$\phi$</th>
<th>$g$</th>
<th>$P$</th>
</tr>
</thead>
<tbody>
<tr>
<td>CM-5</td>
<td>6</td>
<td>2.2</td>
<td>4</td>
<td>512</td>
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<tr>
<td>Meiko CS-2</td>
<td>8.6</td>
<td>1.7</td>
<td>14.2 + 0.03x</td>
<td>64</td>
</tr>
<tr>
<td>Power Xplorer</td>
<td>21 - 0.82x</td>
<td>70 + x</td>
<td>115 + 1.43x</td>
<td>8</td>
</tr>
<tr>
<td>Para-Station</td>
<td>50 - 0.10x</td>
<td>3 + 0.112x</td>
<td>3 + 0.119x</td>
<td>4</td>
</tr>
<tr>
<td>IBM SP-2</td>
<td>13 - 0.005x</td>
<td>8 + 0.008x</td>
<td>10 + 0.01x</td>
<td>128</td>
</tr>
<tr>
<td>IBM SP-2</td>
<td>17 - 0.005x</td>
<td>8 + 0.008x</td>
<td>10 + 0.01x</td>
<td>256</td>
</tr>
</tbody>
</table>
Improving LogP

• First model to break the synchrony of parallel execution
• LogGP: augments the LogP model with a linear model for long messages
• LogGPC model extends the LogGP model to include contention analysis using queuing model on the $k$-ary $n$-cubes network
• LogPQ model augments the LogP model on the stalling issue of the network constraint by adding buffer queues in the communication lines.
The CCM model

- Collective Computing Model transform the BSP superstep framework to support high-level programming models as MPI and PVM.
- Remove the requirement of global synchronization between supersteps, but combines the message exchanges and synchronization properties into the execution of a collective communication.
- Prediction quality usually high.