Homework Assignment

- Implement, in Fortran or C, the six different ways to perform matrix multiplication by interchanging the loops. (Use 64-bit arithmetic.) Make each implementation a subroutine, like:

  - subroutine ijk ( a, m, n, lda, b, k, ldb, c, ldc )
  - subroutine ikj ( a, m, n, lda, b, k, ldb, c, ldc )
  - ...

6 Variations of Matrix Multiple

\[
\text{for } _i = 1:n; \\
\text{for } _j = 1:n; \\
\text{for } _k = 1:n; \\
C_{i,j} \leftarrow C_{i,j} + A_{i,k} B_{k,j} \\
\text{end} \\
\text{end} \\
\text{end}
\]
6 Variations of Matrix Multiple

for _ = 1:n;
    for _ = 1:n;
        for _ = 1:n;
            \( C_{i,j} \leftarrow C_{i,j} + A_{i,k} B_{k,j} \)
        end
    end
end
end
6 Variations of Matrix Multiple

for _ = 1:n;
  for _ = 1:n;
    for _ = 1:n;
      \( C_{i,j} \leftarrow C_{i,j} + A_{i,k} B_{k,j} \)
    end
  end
end
6 Variations of Matrix Multiple

for _ = 1:n;
    for _ = 1:n;
        for _ = 1:n;
            \[ C_{i,j} \gets C_{i,j} + A_{i,k} B_{k,j} \]
        end
    end
end
6 Variations of Matrix Multiple

```plaintext
for _ = 1:n;
  for _ = 1:n;
    for _ = 1:n;
      C_{i,j} ← C_{i,j} + A_{i,k} B_{k,j}
    end
  end
end
```
6 Variations of Matrix Multiple

for _ = 1:n;
    for _ = 1:n;
        for _ = 1:n;
            \[ C_{i,j} \leftarrow C_{i,j} + A_{i,k} B_{k,j} \]
        end
    end
end
6 Variations of Matrix Multiple

```plaintext
for _ = 1:n;
  for _ = 1:n;
    for _ = 1:n;
      C_{i,j} ← C_{i,j} + A_{i,k} B_{k,j}
    end
  end
end
```

![Diagram of matrix multiplications](image-url)
6 Variations of Matrix Multiple

\[
\begin{align*}
C_{i,j} &\leftarrow C_{i,j} + A_{i,k} B_{k,j} \\
\end{align*}
\]

Fortran

```
for _ = 1:n;
    for _ = 1:n;
        for _ = 1:n;
            C_{i,j} \leftarrow C_{i,j} + A_{i,k} B_{k,j}
        end
    end
end
```
6 Variations of Matrix Multiple

Fortran

C

ijk

ikj

kij

kji

jki

jik

However, only part of the story
Matrices in Cache

For a Pentium III 933 MHz (Coppermine processor)
- L1 data cache 16 KB (also has a L1 instruction cache 16 KB)
  \[ \sqrt{16\text{KB}/8} \approx 45 \]
- L2 cache 256 KB
  - \( \sqrt{256\text{K}/8} = 179 \)

For a Pentium III 550 MHz (Katmai processor)
- L1 data cache 16 KB (also has a L1 instruction cache 16 KB)
- L2 cache 512 KB
  - \( \sqrt{512\text{K}/8} = 252 \)
C = C + A*B (Intel Xeon 3.2GHz)