CCDSC’14 Panel

Exascale topic

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- Roadmap not reflective of exact launch granularity and timing – please refer to ILU guidance.
Problem statement (2011)

Today 5kW for 1 TFlops

- Decode and control
- Cache memory
- ... and much more
- Power system inefficiencies
- Cooling
- ... and more

5kW

100W

100W

150W

200W

4450W

10TB disk @ 1TB/disk @10W

100pJ com per FLOP

0.1B/FLOP @ 1.5nJ per Byte

200pJ per FLOP
Problem statement (2011)
ExaFlops ???

1 EF (ExaFlops) = 10^{18} Flops

How can we achieve this?
It *could* take:
- A microarchitecture that does 10 ops/cycle $10^1$
- In a core running at 2GHz $2 \times 10^9$
- With 250 cores per socket $2.5 \times 10^2$
- On a 200,000 sockets $2 \times 10^5$

One among many solutions
ExaFlops ???

1 EF (ExaFlops) = $10^{18}$ Flops

How can we achieve this?
It *could* take:
- A microarchitecture that does 10 ops/cycle
- In a core running at 2GHz
- With 100 cores per socket
- On a 500,000 sockets

One among many solutions
ExaFlops ???

1 EF (ExaFlops) = 10^{18} Flops

How can we achieve this? It *could* take:
- A microarchitecture that does 10 ops/cycle
- In a core running at 1GHz
- With 500 cores per socket
- On a 200,000 sockets

One among many solutions
ExaFlops ???

1 EF (ExaFlops) = $10^{18}$ Flops

How can we achieve this?
It *could* take:
- A microarchitecture that does 10 ops/cycle $10^1$
- In a core running at 1GHz $10^9$
- With 1,000 cores per socket $10^3$
- On a 100,000 sockets $10^5$

One among many solutions
Moore’s Law

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Moore’s Law - 22nm Tri-Gate

3rd Generation Intel® Core™ 
Processor Family 
(2012, codename IvyBridge) 

4,000X Faster 
5,000X Less Energy / Transistor 
50,000X Cheaper / Transistor 

4004 (1971) 

vs. 

Source: Intel